Amendment to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-13 (Canceled)

Claim 14 (Original) A vertical semiconductor device comprising:

a first conductivity type base layer having resistance higher than that of a first conductivity type buffer layer;

said first conductivity type buffer layer formed in one surface portion of said first conductivity type base layer;

a second conductivity type drain layer selectively formed in a surface portion of said first conductivity type buffer layer;

a second conductivity type base layer selectively formed in the other surface portion of said first conductivity type base layer;

a first conductivity type source layer selectively formed in a surface portion of said second conductivity type base layer;

a gate insulating film formed on said second conductivity type base layer between said first conductivity type source layer and said first conductivity type base layer;

a gate electrode formed on said second conductivity type base layer via said gate insulating film;

a drain electrode electrically connected to said second conductivity type drain layer; and

a source electrode electrically connected to said first conductivity type source layer and said second conductivity type base layer,

wherein said drain electrode is not electrically connected to said first conductivity type buffer layer.

Claim 15. (Original) A device according to claim 14, wherein a surface impurity concentration Cs of said second conductivity type drain layer satisfies

$Cs > 1 \times 10^{19}\ cm^{-3}$.

Claim 16. (Original) A device according to claim 14, wherein a barrier metal layer is formed between said drain electrode and said second conductivity type drain layer.

Claim 17. (Original) A vertical semiconductor device comprising:

a first conductivity type base layer having resistance higher than that of a first conductivity type buffer layer;

said first conductivity type buffer layer formed in one surface portion of said first conductivity type base layer;

a plurality of trenches formed in the other surface portion of said first conductivity type base layer;

a second conductivity type base layer formed to be shallower than said trenches, in the other surface portion of said first conductivity type base layer;

a first conductivity type source layer formed on the two sides of each trench, in a surface portion of said second conductivity type base layer;

a gate insulating film formed on the side walls and bottom surfaces of said trenches;

a gate electrode formed via said gate insulating film so as to fill said trenches;

a source electrode electrically connected to said first conductivity type source layer and said second conductivity type base layer;

a second conductivity type drain layer selectively formed in a surface portion of said first conductivity type buffer layer; and

a drain electrode electrically connected to said second conductivity type drain layer,

wherein said drain electrode is not electrically connected to said first conductivity type buffer layer.

Claim 18. (Original) A device according to claim 17, wherein a surface impurity concentration Cs of said second conductivity type drain layer satisfies

$Cs > 1 \times 10^{19}\ cm^{-3}$.

Claim 19. (Original) A device according to claim 17, wherein a barrier metal layer is formed between said drain electrode and said second conductivity type drain layer.

Claim 20. (Original) A vertical semiconductor device comprising:

a first conductivity type semiconductor substrate having resistance higher than that of a first conductivity type buffer layer;

said first conductivity type buffer layer formed in one surface portion of said first conductivity type semiconductor substrate;

a plurality of first trenches formed in the other surface portion of said first conductivity type semiconductor substrate;

a second conductivity type base layer formed to be shallower than said first trenches, in the other surface portion of said first conductivity type semiconductor substrate;

a first conductivity type source layer formed on the two sides of each first trench, in a surface portion of said second conductivity type base layer;

a first insulating film formed on the side walls and bottom surfaces of said first trenches;

a gate electrode formed inside said first trenches via said first insulating film so as to fill said first trenches;

a source electrode connected to said first conductivity type source layer and said second conductivity type base layer;

a second trench formed in said first conductivity type buffer layer;

a second insulating film formed on the side walls of said second trench;

a second conductivity type first drain layer formed in a bottom surface portion of said second trench;

a second conductivity type second drain layer formed to be shallower than said second trench, in a surface portion of said first conductivity type buffer layer;

a buried drain electrode formed inside said second trench via said second insulating film so as to fill said second trench, and connected to said second conductivity type first drain layer; and

a drain electrode connected to said second conductivity type second drain layer and said buried drain electrode.

Claim 21. (Original) A vertical semiconductor device comprising:

a first conductivity type semiconductor substrate having resistance higher than that of a first conductivity type buffer layer;

said first conductivity type buffer layer formed in one surface portion of said first conductivity type semiconductor substrate;

a second conductivity type base layer selectively formed in the other surface portion of said first conductivity type semiconductor substrate;

a first conductivity type source layer selectively formed in a surface portion of said second conductivity type base layer;

a gate insulating film formed on said second conductivity type base layer between said first conductivity type source layer and said first conductivity type semiconductor substrate;

a gate electrode formed on said second conductivity type base layer via said gate insulating film;

a source electrode connected to said first conductivity type source layer and said second conductivity type base layer;

a trench formed in said first conductivity type buffer layer;

an insulating film formed on the side walls of said trench;

a second conductivity type first drain layer formed in a bottom surface portion of said trench;

a second conductivity type second drain layer formed to be shallower than said trench, in a surface portion of said first conductivity type buffer layer;

a buried drain electrode formed inside said trench via said insulating film so as to fill said trench, and connected to said second conductivity type first drain layer; and

a drain electrode connected to said second conductivity type second drain layer and said buried drain electrode.